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DESIGN AND IMPLEMENTATION OF HIGH SPEED LATCHED COMPARATOR USING g_m/I_d SIZING METHOD

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Abstract

Design of an analog circuit depends on several factors such as design methodology, good modeling and technology characterization. This work focuses on designing a high speed (1.6GHz) latched comparator with low power consumption suitable for ADCs in SoC applications. The latched comparator is designed with StrongArm latch as the primary decision and amplification stage followed by a latching element to drive the output load. The StrongArm latch is a proven circuit topology suitable for all seasons. The zero static power consumption of StrongArm latch is exploited to design a low power comparator. The output latch is used to hold the previous output value during the tracking time of the comparator. The designed comparator achieves zero setup time at a clock frequency of 1.6GHz and produces digital output with a maximum delay of 180ps.The comparator is implemented with SAED 32nm technology libraries. The performance has been analyzed using HSPICE simulator.

Keywords:

Latched Comparator, Strong Arm Latch, High Speed, Low Power

1. INTRODUCTION

Comparator finds its applications as zero detector, voltage comparator etc. The primary area of application of comparators is Analog to Digital Converters. The number of comparators in an ADC increases as the resolution of ADC increases. Hence the power consumption of ADC can be reduced by utilizing a low power comparator. But at the same time to fulfill the tight timing constraints of the ADC the speed of the comparator should also be taken care while designing. Conventional comparator structure [1] uses three stages to produce the final output. It suffers from large static power consumption since the pre-amplifier stage continuously amplifies the input differential signal. So it cannot be employed for low power applications. The static power consumption depends on the tail current of the current source used in the amplifier stage [2]. The StrongArm latch proposed in [3] controls static power dissipation by clocking the tail current source. And it also produces full scale output swing. These advantages of StrongArm latch make it suitable for low power applications.

The StrongArm latch is reset for every clock cycle. So a RS latch is used to hold the output value until the StrongArm latch produces the output for the next clock cycle.

In this work the g_m/I_d design methodology proposed by [4] is used to size the transistors. It is a unified synthesis methodology in all regions of operation of the MOS transistors.

The paper is organized as follows. Section 2 gives operation principle of StrongArm latch. Section 3 describes the architecture of RS latch used in this work. Section 4 addresses the g_m/I_d sizing methodology applied in this work. Section 5 shows the simulation results. Finally section 6 presents our conclusions.

2. OPERATION OF STRONGARM LATCH

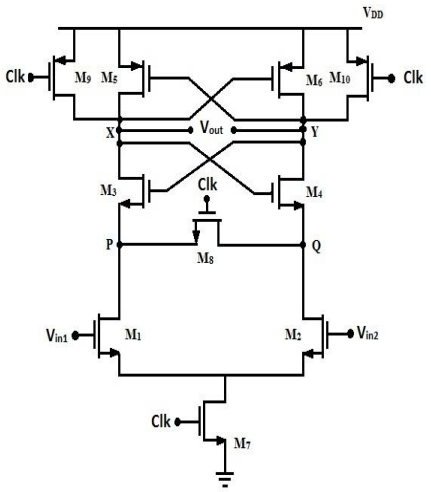

Fig.1. StrongArm latch circuit topology

The Fig.1 shows the StrongArm latch circuit topology. It consists of an NMOS differential pair (M_1-M_2), two cross coupled pairs (M_3-M_6), tail current source (M_7), pre-charge switches (M_9-M_{10}) and an additional transistor (M_8).

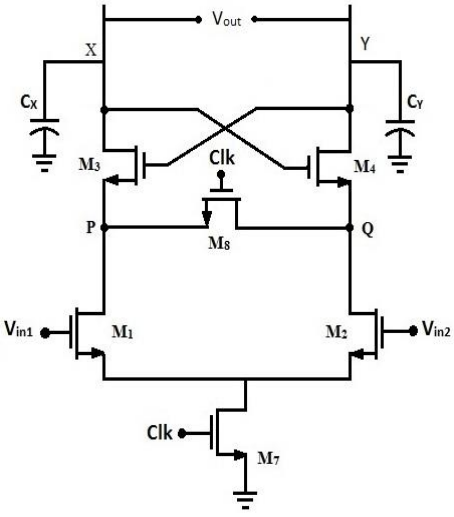

Fig.2. Precharge Phase

The circuit operation can be divided into following phases. When *CLK* is low the pre-charge switches are turned on. Since there is no DC path to ground it charges the nodes *X* and *Y* to $V_{DD,}$ which makes the NMOS pairs (M_3-M_4) to turn on. Consequently the nodes *P* and *Q* are also precharged to V_{DD}. Since any of the transistors M_1

or M_2 is turned on, the common node between M_1, M_2 and M_7 is precharged to V_{DD}-V_{tn}. Thus all the capacitances in the structure are precharged (Fig.2). This is called precharge phase.

In the second phase, the CLK goes high, the precharge switches (M_9-M_{10}) are turned off and M_1 and M_2 turned on drawing a differential current proportional to the applied potential difference (V_{in1}-V_{in2}). This current flows from the precharged capacitances in the first phase (C_X, C_Y). If V_{in1}>V_{in2}, then the transistor M_1 draws more current. So the voltage at node X discharges through M_3, M_1, and M_7. Similarly if V_{in1}<V_{in2}, then the transistor M_2 draws more current. So the voltage at node Y discharges through M_4, M_2, and M_7 (Fig.3(a) and Fig.3(b)). This differential current flow allows $|V_x$-$V_Y|$ to grow and exceed $|V_{in1}$-$V_{in2}|$. This phase provides differential gain, and so, called as amplification phase.

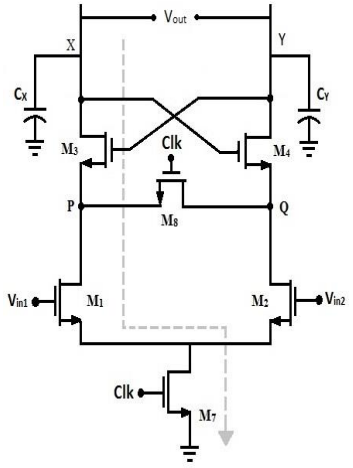

Fig.3(a). Current discharge through capacitors (Clk = 0& V_{in1}> V_{in2})

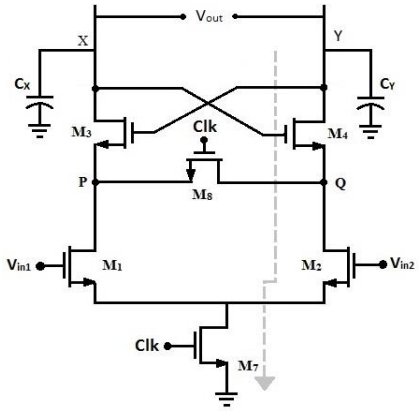

Fig.3(b). Current discharge through capacitors (Clk = 0 & V_{in1}> V_{in2})

Due to the current drawn by the differential pair, the voltages V_x and V_Y continue to fall until it reaches V_{DD}-V_{tp} making either of the transistor pair (M_5-M_6) turn on. This makes any of the nodes X or Y to fall to zero while letting the other node to reach V_{DD}. Thus the primary decision of comparison is taken in this phase.

All the transistors in the StrongArm latch are of equal importance. The transistors M_3-M_4 cut off the DC path to ground during the final phase which avoids static power drain through tail current source. The transistors M_5-M_6 restore the output nodes (X,Y) to V_{DD}. Without them we only get degraded output high if the input difference $|V_{in1}$-$V_{in2}|$ is small. The precharge switches (M_9-M_{10}) serve two purposes.

- It clears the previous output values at nodes X and Y for every clock cycle. This is called resetting.
- Establishes an initial voltage of V_{DD} at nodes X and Y and ensures the transistors M_5-M_6 remain off prior to the amplification phase. This allows rail-to-rail swinging at the output terminals of StrongArm circuit.

The StrongArm latch produces invalid outputs for half of the clock cycle. Hence an RS latch should follow the StrongArm circuit to interpret the output correctly. The Fig.4 shows the circuit topology used to form the latched comparator.

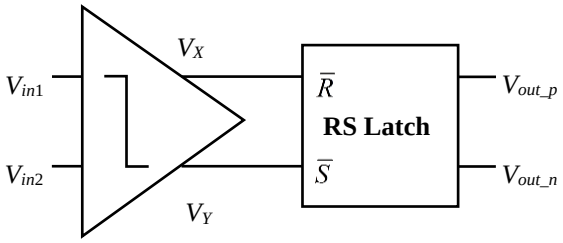

Fig.4. Latched comparator block diagram

3. RS LATCH

RS latch is used to hold output data during precharge phase. Conventional RS latch (Fig.5) suffers from a non-symmetry in the output.

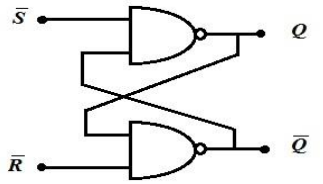

Fig.5. Conventional RS latch

The RS latch has two inputs $\overline{S}$ (Set) and $\overline{R}$ (Reset). Low level at both the inputs is not allowed and that is guaranteed by StrongArm latch. A low level input at $\overline{S}$ makes Q output high and forces $\overline{Q}$ to low. Similarly a low level input at $\overline{R}$ makes $\overline{Q}$ output high and forces Q to low. Thus, at any condition one of the outputs is always delayed with respect to other. To overcome this non-symmetry the modified RS latch shown in [4] is used in this work. Symmetry can be achieved by making the outputs Q and $\overline{Q}$ independent of each other. So the following output expression which only uses the inputs and present states are used to implement RS latch.

Let's say Q^+ and $\overline{Q}^+$ represents the next states of Q and $\overline{Q}$.

$$Q^+ = S + \overline{R} \cdot Q \quad (1)$$

$$\overline{Q}^+ = R + \overline{S} \cdot \overline{Q} \quad (2)$$

The Eq.(1) is implemented as an AND–OR structure, where S is an OR branch. Similarly the same topology applies for Eq.(2) also. These expressions are used to reduce the number of P type transistors which is responsible for transition from 0 to 1. The Fig.6

shows the latch circuit resulting from the above expressions.

The latch has the following advantages.

- During the state change only one transistor in the latch is active which allows the usage of small keeper transistors (M_5-M_{12}).
- The symmetrical structure of the circuit provides equal delay for both the outputs.

The small sized keeper transistors turned off quickly during the transition which allows the driver transistor (M_1-M_4) to change the state of the latch and to drive the load effectively. So based on the load of the following stage the driving transistors can be sized straight forwardly. In this modified RS latch both the true and complimentary outputs have the same drive strength and equal delay which is more important for the latched comparator application.

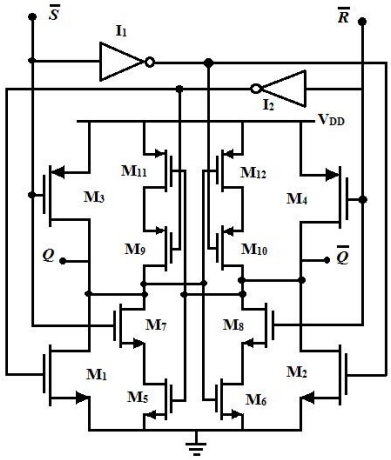

Fig.6. New RS latch

4. g_m/I_d SIZING METHODOLOGY

The conventional synthesis methodologies for analog circuits assume transistors to be in either strong inversion or in weak inversion. But, g_m/I_d is a unified synthesis methodology in all regions of operation of MOS transistor.

This method of sizing exploits the relationship between the ratio of the transconductance (g_m) over the drain current ratio and the normalized current ($I_d/(W/L)$).

The g_m/I_d method is used because of the following reasons.

- It is directly related to the device operating region.
- It can be used to determine the device aspect ratio.
- It is more related to the performance of analog circuits.

The relationship between g_m/I_d and $I_d/(W/L)$ is unique for all transistors of same type for a given technology. The relationship from the curve g_m/I_d vs. $I_d/(W/L)$, can be exploited to determine the transistor aspect ratio when dimensions are unknown.

The Fig.7 shows the curve g_m/I_d versus $I_d/(W/L)$ obtained by HSPICE simulation using SAED 32nm technology models. Once the device operating region is decided (i.e. if g_m/I_d is fixed) then the normalized current and device size can be obtained from the curve shown in Fig.7, Fig.8 and Fig.9 will assist in selecting the appropriate g_m/I_d value. Selecting a higher g_m/I_d value will make the amplification gain of the transistor high at a significant cost improvement in terms of area. So the tradeoff between amplification gain and size of the transistor should be considered while choosing the g_m/I_d value.

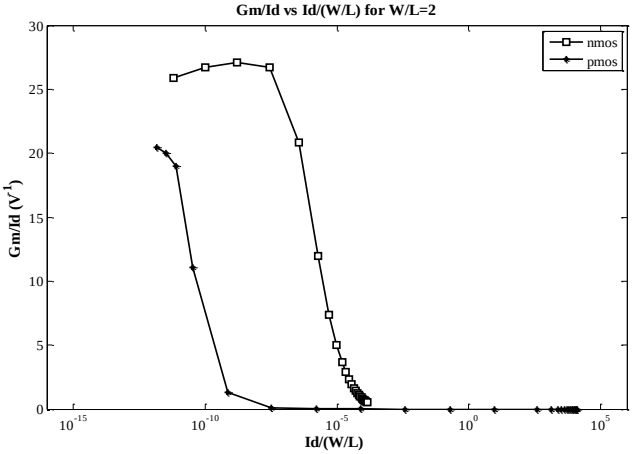

Fig.7. g_m/I_d versus $I_d/(W/L)$ curve for SAED 32nm technology model

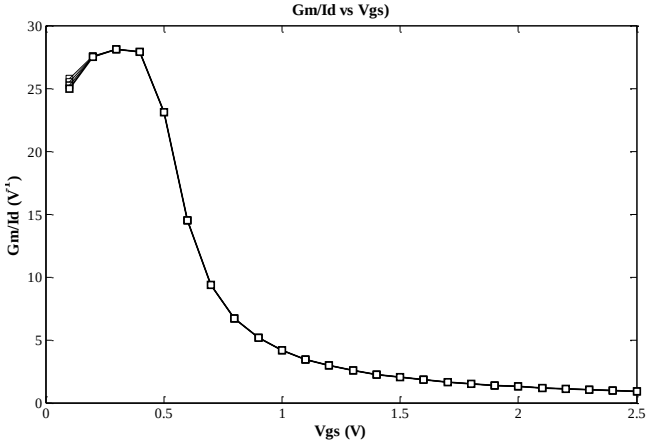

Fig.8. Graph showing relationship between g_m/I_d and V_{GS}

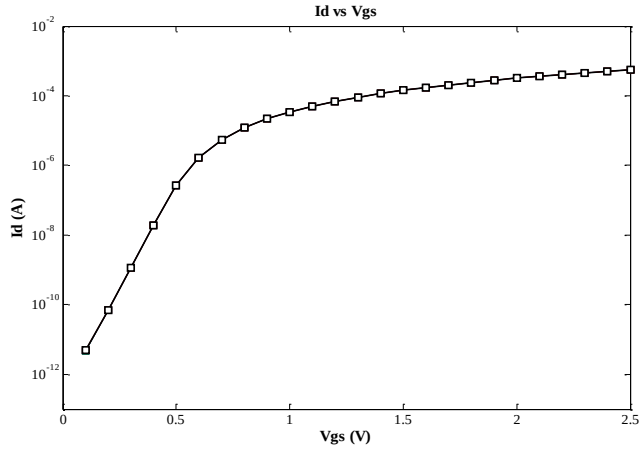

Fig.9. Graph showing relationship between I_d and V_{GS}

The g_m/I_d methodology is applied to the StrongArm latch to attain the specifications shown in Table.1.

Table.1. Targeted specifications

Parameter	Lower bound	Upper bound	Description
V_{INCM}	0.2V	1.2V	Input common mode voltage
V_{INDIFF}	150mV	250mV	Input differential voltage
F_{IN}	-	1.6GHz	Maximum frequency
V_{INTRF}	50ps	100ps	Input rise and fall time.
V_{HIST}	-	50mV	Input hysteresis range
C_{LOAD}	-	20fF	Maximum capacitive load

In addition to the above specifications maximum operating mode power consumption is limited to 5mW with supply voltage of 2.5V.

The main differential pair transistors are operated in strong inversion region to ensure high gain during amplification phase. At the same time the maximum power consumption limitation of 5mW is accomplished. Making the transistor sizes bigger will increase the value of Precharge capacitances of the StrongArm circuit, which leads to higher power consumption. To reduce this we choose $(g_m/I_d)_1 = (g_m/I_d)_2 = 10$.

The tail current source transistor (M_7) should be capable of discharging the main differential pairs. Furthermore, also to maintain the tail source in saturation region of operation the $(g_m/I_d)_7$ is chosen between 5 and 10. Similarly the ratios for other transistors were chosen based on their operating region. Finally, the aspect ratio (W/L) of the devices was calculated approximately using the (g_m/I_d) curves. And upon sequence simulations the transistor sizes were tweaked to attain the targeted specifications. The Table.2 lists the transistor widths and lengths used in this simulation.

Table.2. Transistor Dimensions

Transistor	Width(µm)	Length(µm)
M_1	28.8	0.26
M_2	28.8	0.26
M_3	4.32	0.26
M_4	4.32	0.26
M_5	9	0.26
M_6	9	0.26
M_7	57.6	0.26
M_8	28.8	0.26
M_9	3.6	1.04
M_{10}	3.6	1.04

5. SIMULATION RESULTS

The comparator formed using StrongArm latch and RS latch is simulated using the test bench shown in Fig.10 with a supply voltage of 2.5V to ensure its reliable operation and its output is shown in Fig.11. Comparator is clocked with a 2GHz clock and a 20fF capacitive load is used for simulation.

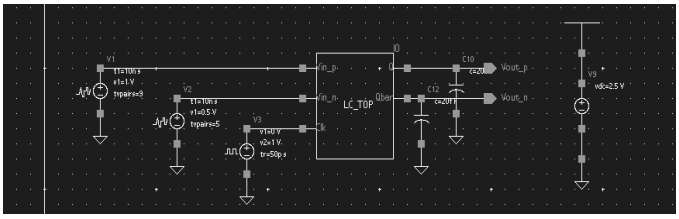

Fig.10. Test bench for Latched Comparator

The Fig.12 shows the Delay and Slew rate of the comparator. The small clk to output delay of 104.88ps makes it suitable for high speed ADC applications.

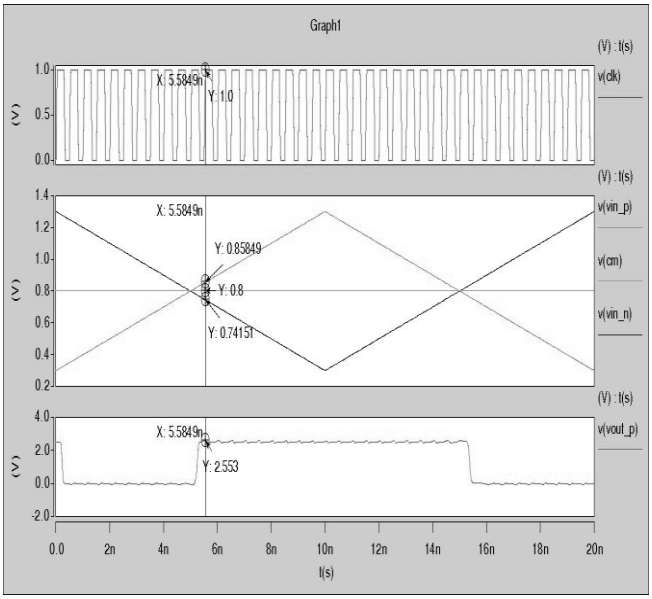

Fig.11. Output of comparator @2GHz clock

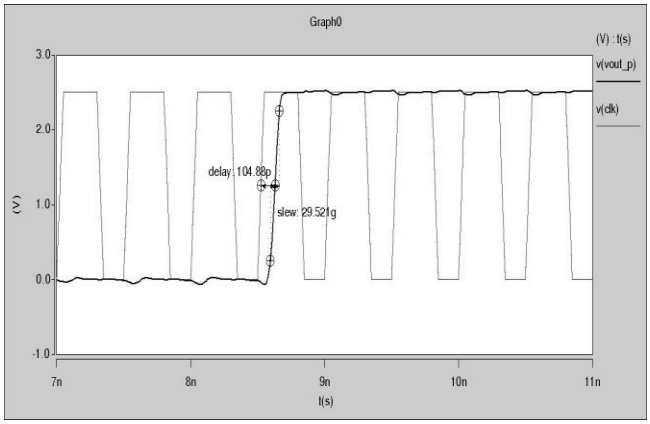

Fig.12. Delay and Slew rate of the comparator

To further ensure the robustness of the design the comparator is simulated at different process corners and at different common mode voltage (V_{cm}). The obtained results are listed in Table.3.

Table.3. Comparator Characteristics at Different Corners

Corners	TT	FF	SS
V_{hist}(mV)	100	100	100

T_{setup}(pS)	311	304	331
T_{hold}(pS)	778	778	803
T_{delay}(pS)	254	253	291
P(mW)	1.905	2.112	1.737
PDP(pJ)	0.484	0.534	0.50547

Table.4. Comparator Characteristics at Different V_{cm}

Common mode voltage V_{cm}(V)	**0.4**	**0.6**	**0.8**	**1.0**	**1.2**
V_{hist}(mV)	580	90	100	100	100
T_{setup}(pS)	357	390	382	321	311
T_{hold}(pS)	942	700	679	800	778
T_{delay}(pS)	180	369	303	286	254
P	475uW	1.44mW	1.62mW	1.770mW	1.905mW
***PDP*(pJ)**	0.0855	0.53136	0.49086	0.50622	0.48387

The Table.4 lists the comparator characteristics measured at different common mode voltages. The Power Delay Product can be taken as a good figure of merit to analyze the energy consumed by the comparator during the switching event. The Table.4 shows that the energy consumed by the comparator is almost equal for different common mode voltages. This implies that the StrongArm consumes zero or very less static power (which is the major power dissipating component in the presence of common mode voltage).

Table.5. Comparison

Reference	**Technology**	**Supply Voltage**	**Power**	**Speed**
[1]	180nm	1.8V	102uW	125MHz
[6]	90nm	1.2V	360uW	100MHz
[7]	32nm	1V	6.4nW	500MHz
StrongArm	32nm	2.5V	1.6mW	2.5GHz

In Table.5, a comparison has been made with the earlier technologies and with other designs of comparator. In work [7] even though low power consumption is achieved at a lower clock frequency, the switching happening at output nodes as well as at the f_n and f_p nodes. It doubles the switching for every comparison. It increases the energy consumption over a long duration. And also the supply needs to charge and discharge the capacitances from supply long way through ground. The StrongArm circuit masters the above drawbacks.

6. CONCLUSION

The large power dissipation problem of conventional comparators has been alleviated by the use of StrongArm latch. When compared with other comparator architectures the pre-amplification and primary decision is done by a single stage (StrongArm circuit) that reduces the overall area too. This type of high speed comparator can be used in ADCs that require high sampling rate. The obtained results have proven that the Strong Arm latch is suitable for all seasons as mentioned by Razavi [5].

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