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A HIGH GAIN AND LOW NOISE CMOS GILBERT MIXER WITH IMPROVED LINEARITY BASED ON MGTR AND SWITCHED BIASING TECHNIQUE

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Abstract

This brief presents the design of an improved linear Gilbert mixer with high conversion gain and low noise figure by using multiple gated transistor (MGTR) and switched biasing technique. This mixer operates at a radio frequency (RF) of 2.4GHz with a local oscillator (LO) power of 5dBm in UMC 180nm process. The MGTR method is used to increase the linearity of the proposed mixer by the parallel combination of transconductance stage transistors and auxiliary transistors. The switched biasing technique is adopted for a current source instead of static biasing which lowers the noise figure. The integration of two techniques result in a conversion gain (CG) of 10.9dB and a noise figure (NF) of 7.2dB with the third order input intercept point (IIP3) of 10.79dBm. This proposed mixer circuit consumes 4.2mW power from a supply voltage of 1.8V.

Keywords:

Conversion Gain, Gilbert Mixer, MGTR, Noise Figure, Static Biasing

1. INTRODUCTION

Today, there is a great crash on analog and RF systems due to the CMOS technology scaling. In the wireless communication system, RF integrated circuits (RFICs) have much demand due to the promising low cost and low power operation in the frequency range of 2.4GHz. The combination of low noise amplifier (LNA), mixer, voltage controlled oscillator (VCO) and power amplifier (PA) constitute the RF front end design [1]. The mixer is a three port element, which consists of two input signals (RF and LO) and one output signal called the intermediate frequency (IF) signal as shown in the Fig.1. Gilbert cell mixers [2] are broadly used due to their practical conversion gain, linearity, isolation and noise figure among the active mixers. The linearity of mixer is very crucial, as the improvement in linearity of the overall system depends on it. To improve the linearity of the mixer, many techniques and structures have been inovated. Use of these techniques result in complex circuit with high power consumption, more noise and higher cost [3]-[7].

The feedback method [8] is used for circuit's linearization, but it results high dc power consumption and low conversion gain. The linearity of the low noise amplifier (LNA) design is improved by using differential multiple gated transistors (DMGTRs) [9], where it consumes more dc power. The cross coupled post distortion (CCPD) technique [10] enhances the mixer linearity with the drawbacks of high noise figure and low conversion gain. The switched biasing technique [11] is used to reduce the noise originating at tail current source with a dc level shifter. But it desires high supply voltages due to the use of more number of transistors.

In this work, both the MGTR and switched biasing techniques are used together in the design of the mixer to attain high gain, improved linearity and low noise figure in 0.18µm CMOS technology. The noise figure for this design is 7.2dB and it achieves the conversion gain of 10.9dB. The proposed mixer circuit works at a supply voltage of 1.8V and it consumes 4.2mW power with the IIP3 of 10.79dBm.

The section 2 explains the design of proposed mixer with MGTR linearization and switched biasing techniques. The section 3 represents the simulation results with the comparison table. Finally, it is concluded in section 4.

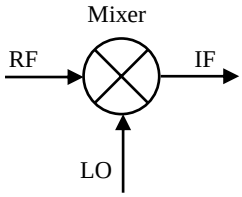

Fig.1. Mixer Symbol Representation

2. DESIGN AND ANALYSIS OF PROPOSED MIXER CIRCUIT

The important performance measurement of the Gilbert type mixer is the linearity, which is determined primarily by its transconductance stage. Here the MGTR technique is used to improve the linearity of the mixer circuit. At the cost of high power consumption and moderate conversion gain, we can achieve the high linearity of the mixer. At the same time, the noise figure is increased while keeping the conversion gain intact. To overcome this problem of higher noise figure, the switched biasing technique with a DC level shifter is combined with the MGTR technique.

2.1 MGTR LINEARIZATION TECHNIQUE

By Taylor series expansion, a common source drain current with respect to gate to source voltage (V_{gs}) is represented in the Eq.(1) [12].

$$I_{DS} = I_{DC} + g_m V_{gs} + \frac{g_m^{'}}{2!} V_{gs}^2 + \frac{g_m^{''}}{3!} V_{gs}^3 + \ldots \quad (1)$$

where, g_m^n represents the n^{th} order derivatives of the transconductance.

The Linearity of mixer is calculated by IIP3, which is explained in Eq.(2) [12]-[13]

$$\text{IIP3} = \sqrt{\frac{4}{3}\frac{\alpha_1}{\alpha_2}} \quad (2)$$

where,

$$\alpha_1 = g_m ,$$

$$\alpha_3 = \frac{g_m^{''}}{3!}$$

α_1 and α_2 are the coefficients of non-linearity.

The Fig.2 represents the schematic of MGTR technique, which consists of T1, T2, T1a and T2a nMOS transistors. T1 and T2 are the main transistors, which provide major mixer gain. T1a and T2a are the auxiliary transistors, which improve the linearity of the mixer circuit.

The input signal (RF) is applied to all the transistor's gate terminals. The drain of T1 (T2) transistor is connected with the drain of the T1a (T2a) transistor. The auxiliary transistors (T1a, T2a) operate in weak inversion region and the main transistors (T1, T2) operate in the saturation region. The MGTR technique cancels the third order derivative from the Eq.(1) due to the T1a and T2a transistors. The linearity is enhanced by auxiliary transistors, by cancelling the negative peak value of $g_m^{"}$ of the T1 and T2 transistors with the positive peak value of $g_m^{"}$ [13]. This MGTR method does not get through any extra power as the auxiliary transistors operate in sub threshold region [9], [14].

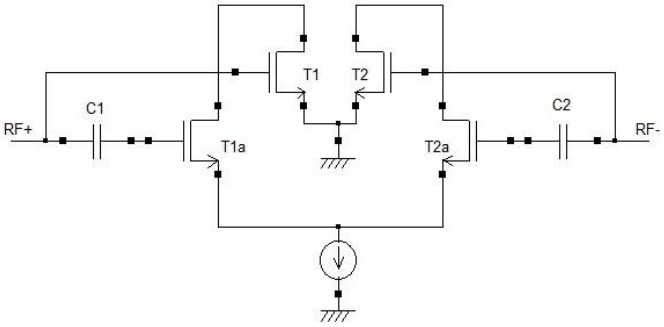

Fig.2. Schematic of MGTR

2.2 SWITCHED BIASING TECHNIQUE

The Fig.3 shows the schematic of the switched biasing technique, in which the tail current source divides into two half size nMOS transistors (M1 and M2).

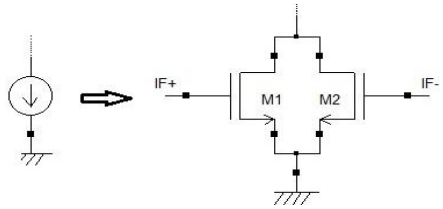

Fig.3. Tail Current Source to Transistor Representation

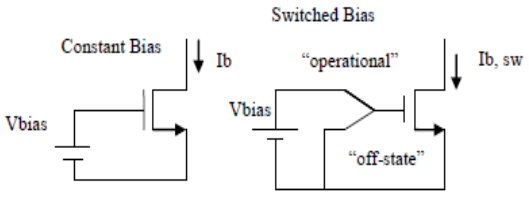

Fig.4. Operation of Switched Biasing Technique

The operation of the switched biasing technique is explained in Fig.4. Here, both transistors are periodically switched in "operational" state and "off-state". The "operational" state works in saturation region to provide a constant bias current *Ib*, whereas the "off-state" operates below threshold to overlook about its last flicker noise performance [11]. Hence, the noise figure is improved as compared to the static biasing current source [14].

2.3 DESCRIPTION OF PROPOSED MIXER

The schematic diagram of the proposed mixer is given in Fig.5. It includes an active load stage (M1-M2), LO switching stage (M3-M6), RF transconductance stage (M7-M8) with the auxiliary transistors (M9-M10) and the switched biasing stage (M11-M12) with a dc level shifter (M13-M14 and RB). The transconductance stage converts RF voltage to RF current and the IF current is converted from RF current by the switching stage. The M1 and M2 pMOS transistors are used for impedance matching purpose and it changes IF current to IF voltage.

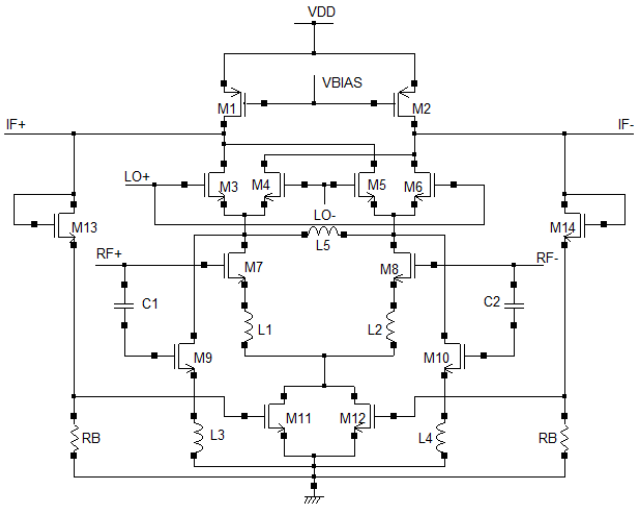

Fig.5. Proposed Mixer Schematic

In MGTR technique, two auxiliary transistors M9 and M10 is linked with the two main transistors M7 and M8 in the transconductance stage (g_m). Here, the drains of M7 and M8 transistors are coupled to the respective drains of M9 and M10 transistors. The inductors L1, L2, L3 and L4 at the source of main and auxiliary transistors are used for impedance matching purposes. For tunning of the parasitic capacitors, an inductor L5 is inserted in between two trasconductance stages, which improves the conversion gain of the mixer. C1 and C2 are used as the dc blocking capacitors. The main transistors (M7-M8) operate in the saturation region with a negative peak value of $g_m^{"}$, whereas the auxiliary transistors (M9-M10) work in the sub threshold region with a positive peak value of $g_m^{"}$, which cancels the 3rd order nonlinearity of the nMOS transistor. As a result, there is enhancement in IIP3 which improves the linearity performance. The MGTR technique also exhibits good conversion gain, but high noise figure.

The transistors (M3-M6) are used for the switching operation, in which the high flicker noise is passed to the output during the on / off transition at the time of mixing. To reduce the flicker noise, the switched biasing technique is used. Here, two half size transistors (M11-M12) are replaced by the tail current source, which are alternately switched by the output signals. The flicker noise is reduced by the operation of M11 and M12 transistors in between saturation and accumulation regions, which release trapped charge carriers. A dc level shifter (M13, M14 and RB) is

implemented for the symmetric switching operation of M11 and M12 transistors with a proper gate to source voltage [11]. It results low overdrive voltage with a small output swing, which improves the noise figure.

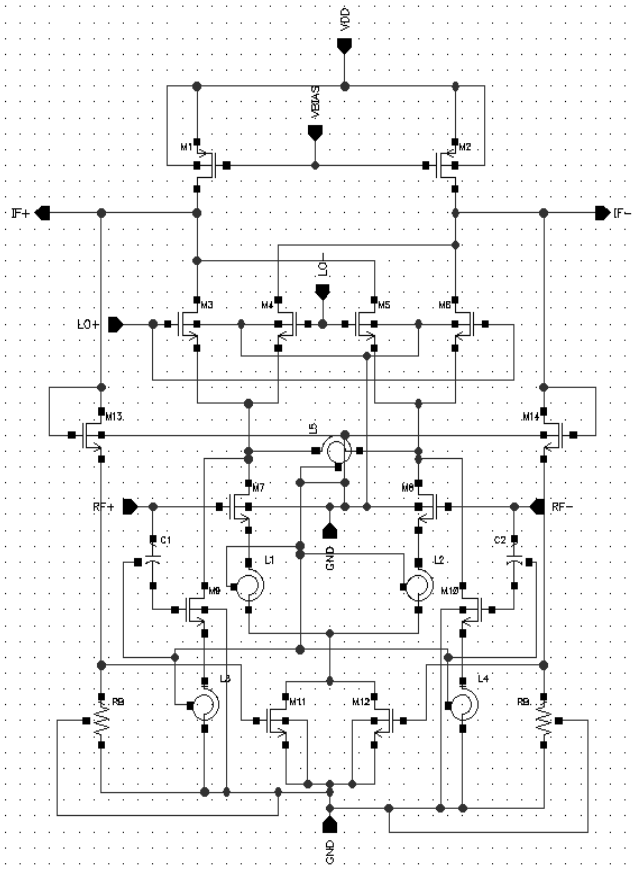

Fig.6. Proposed Mixer Schematic in Cadence Tool

3. SIMULATION RESULTS AND DISCUSSION

Simulation of the proposed mixer is carried out with the UMC cadence tool in 0.18 µm CMOS process and the schematic is shown in Fig.6. The Fig.7 shows the transient analysis of the proposed circuit, in which the IF frequency is calculated as 100MHz with respect to 2.4GHz RF frequency.

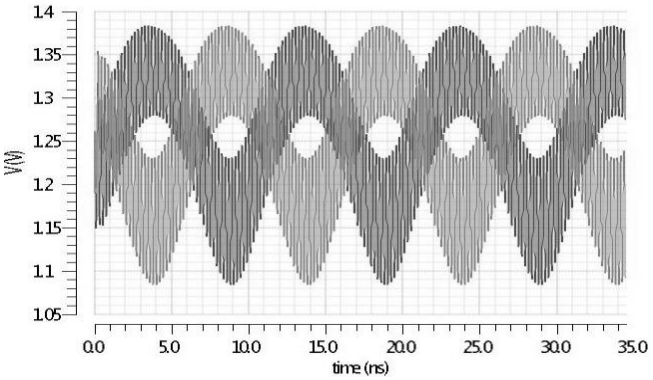

Fig.7. Transient Analysis of Proposed Mixer

The Fig.8 represents the graph between conversion gain and LO power. Here, the maximum conversion gain is observed as 10.9dB at a LO power of 5dBm and the graph decreases with the increase value of LO power.

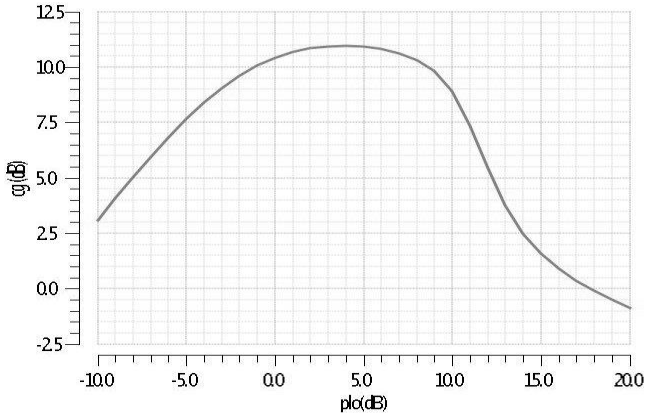

Fig.8. Conversion Gain Versus LO Power

The IIP3 plot of the proposed mixer is shown in the Fig.9. From the graph the IIP3 is obtained as 10.79dBm, which improves the linearity of the proposed mixer.

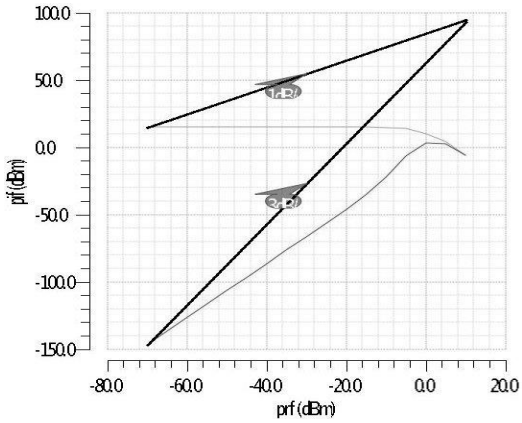

Fig.9. IIP3 of Proposed Mixer

The Fig.10 shows the plot of the noise figure versus IF frequency. The noise figure of the proposed mixer is reduced with the increase frequency value and it is approximately 7.2dB in the 100MHz IF frequency range.

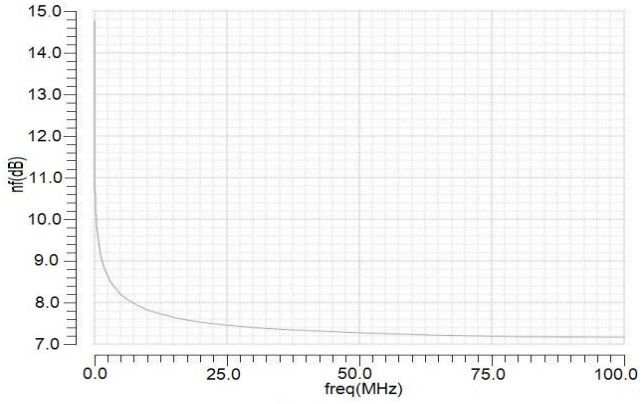

Fig.10. Noise Figure Versus IF Frequency

From the simulation results, it is found that the proposed mixer operates at a supply voltage of 1.8V with 4.2mW power consumption. The conversion gain is 10.9dB, while the IIP3 and the noise figure are 10.79dBm and 7.2dB respectively. In comparison to other CMOS mixers reported in Table.1, the proposed mixer using the combination of MGTR technique and switched biasing technique provides high conversion gain, high linearity and low noise figure. The performance summary of CMOS mixers is shown in the Table.1.

Table.1. Performance Summary of CMOS Mixers

References	[3]	[4]	[7]	[11]	[12]	This Work
Process (μm)	0.25	0.18	0.18	0.18	0.18	0.18
F_{RF} (GHz)	1.9	2.4	2.4	5.8	2.4	2.4
F_{LO} (GHz)	1.85	2.1	2.3	5.9	2.1	2.3
LO Power (dBm)	-	-	-7	0	5	5
IIP3 (dBm)	5.13	8.03	5.46	-5	14.2	10.79
Conversion Gain (dB)	2.13	10.7	3.3	7.5	9.11	10.9
Noise Figure (dB)	18.2	16	14.87	7.6	13.82	7.2
Supply Voltage (V)	2.5	1.8	1.5	1.8	1.8	1.8
Power consumption (mW)	13.01	14.3	5.6	8.1	4.46	4.2

4. CONCLUSION

In this paper, a high gain, low noise figure and improved linear mixer is presented by using 0.18μm CMOS process. The MGTR technique improves the linearity of the mixer circuit by adding auxiliary transistors with a good conversion gain. The low noise figure is obtained with the help of the switched biasing technique with a dc level shifter. The simulation results of the proposed mixer give a minimum noise figure of 7.2dB, the maximum conversion gain of 10.9dB, and IIP3 of 10.79dBm with the power consuming of 4.2mW from 1.8V supply voltage. So, the proposed mixer circuit with high linearity, high gain and improved noise performance may serve as an appropriate block in RF receiver front end design.

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