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DESIGN AND READ STABILITYANALYSIS OF 8T SCHMITT TRIGGER BASED SRAM

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Abstract

This paper presents an 8T Schmitt Trigger (ST) based SRAM design to improve the read stability and power dissipation of conventional 6T SRAM cell. The ST based SRAM cell incorporates built-in feedback mechanism in order to attain robust read operation. The read stability of the cell is 2.5× higher than that of 6T SRAM cell at 1.8V and it can retain data even at a lower Vmin of 0.3V. Also, power consumption is reduced by 22% compared to 6T SRAM design. The layout drawn using 120nm technology rule shows that the 8T ST SRAM occupies 1.2× higher area compared to 6T SRAM cell. Peripheral circuits for the 8T ST SRAM are introduced. Except the precharge circuit and basic SRAM cells, the remaining part of the circuitry is same for both single bit 6T and 8T ST SRAM array design. The single bit 8T ST SRAM array consumes less power and area in nano-scaled technologies. The proposed design was simulated in Mentor Graphics ELDO using TSMC 180nm technology.

Keywords:

Low Voltage SRAM, Schmitt Trigger, Read Stability, Read SNM

1. INTRODUCTION

Over the last few years, feature size of CMOS devices has been dramatically scaled to smaller dimensions. Memories are integral part of most of the digital devices and thus design of VLSI memories has become highly desirable. During the last decade, low power and robust memory designs have drawn great research attention. SRAM has become a crucial component in the memory hierarchy of most of the embedded devices as it dominates the overall performance of the system. SRAM is widely used in many microprocessors and Systems On Chips (SOC) due to its speed and low power consumption.

With supply voltage scaling it can reduce dynamic power quadratically and leakage power exponentially. However, with miniaturization of devices, the impact of process variations influences the Static Noise Margin of the SRAM cell adversely. Since SNM is linearly dependent on supply voltage, scaling down to save power degrades the cell stability. Thus for successful SRAM operation, the stability of the cross coupled inverter is relevant [1][2]. However, the design of robust SRAM faces many process and performance related challenges. With each technology generation as the device size is scaled, random process variations significantly degrade the SRAM cell data stability. This limits the SRAM operation in low-voltage regime employing minimum-sized transistors.

The adoption of supply voltage scaling enable the SRAM bit cell to operate in wide voltage range [3]. But the read stability of conventional 6T SRAM cell degrades to unacceptable level and it is difficult to balance the read stability requirements by delicate transistor sizing. Thus Power, density and read stability of the SRAM cell have become the key limitations in many designs as nano-scaled devices are becoming a reality. Several designs have been used to enhance the stability of the cell for robust low voltage operation. In this paper, 8T Schmitt Trigger based SRAM cell with built-in feedback mechanism is used in order to attain high read stability and to reduce total power dissipation.

The remainder of this paper is organized as follows. Section 2 describes various SRAM cell topologies. Section 3 and section 4 presents a brief review of conventional 6T and 8T SRAM cells. Section 5 presents 10T ST based SRAM cell. In Section 6, the proposed 8T ST SRAM design is discussed. Section 7 presents the simulation results. Finally, conclusion is drawn in section 8.

2. LITERATURE SURVEY

Different configurations of SRAM cells have been proposed to meet various requirements like stability, bitcell area and low voltage operation. In loadless 4T SRAM bitcell [4], PMOS act as access transistors. Here, for maintaining data “1” reliably, PMOS OFF state current should be more than NMOS pulldown leakage current. Satisfying this design requirement over different process, voltage and temperature (PVT) conditions may be challenging. In [5], an asymmetric 5T SRAM cell with single bitline was proposed. It requires dc-dc converters and separate precharge voltages for read and write operations. Additional design margins for bitcell sizing are required to track the read precharge voltage across PVT corners and this limits its application. The conventional 6T achieves large storage capability yet it suffers from Read failure and at low supply voltages its stability degrades to unacceptable level.

In [6], a single ended 6T with transmission gate as access transistors was introduced such that write ability can be improved by modulating virtual VCC and virtual VSS of one of the inverters. The Single ended 7T bitcell proposed in [7] consists of separate single ended write and read ports. The write operation in this single ended 7T bitcell requires either differential VSS/VCC or asymmetrical inverter characteristics. In [8], to address the problem of data storage destruction during read operation, 8T bitcell topology was introduced. It consists of separate read and write ports to retain high read stability.

However, it suffers from read bitline leakage problem and exibit area penality of 30% compared to 6T SRAM cell. In single ended 9T bitcell, stacked read access transistors are used to reduce the bitline leakage current [9]. Single ended 10T bitcell proposed in [10] use the modified version of read path that reduces the bitline leakage and enhance read stability. In [11], a read disturb free differential 10T bitcell with two series connected transistors in write path was introduced. However it degrades the write ability of the cell and requires write assist circuits for a successful write operation.

None of the above bitcells address process variation tolerance at low supply voltages. Thus stability of the cross coupled inverter

pair is very important for successful operation under PVT variations. Therefore in this paper, we propose an 8T Schmitt Trigger based SRAM design which offers high RSNM, reduced power consumption and robustness to PVT variations.

3. CONVENTIONAL 6T SRAM CELL

In conventional 6T SRAM cell, cross coupled inverter is used as the basic element for data storage as shown in Fig.1. It consist of six transistors where the four transistors (M1, M2, M3 and M4) forms the cross coupled inverters and AX1/AX2 are used as the access transistors to control the access to the SRAM cell. During read operation, the bitlines BL and BLB of the cell are pre-charged high and the word line is asserted. When WL is raised, either BL or BLB pulls down indicating the stored data. The read operation results in the formation of voltage divider network that consist of access and pull down transistors and thereby increases the voltage in the node storing logic '0'. This unintended change in the stored state of the cell during read operation is defined as read failure [12].

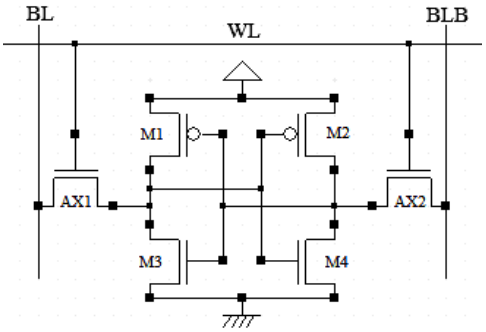

Fig.1.Conventional 6T SRAM cell

The conventional 6T SRAM cell is thus unstable and fails to meet the operational requirements due to reduced Read Static Noise Margin (RSNM). As the RSNM is very low, it is not acceptable for most memory designs especially for low power supply voltages.

4. 8T SRAM CELL

8T cell structure was proposed to overcome the problem of read failure in 6T SRAM cell during read operation. To improve the RSNM, it uses separate read and write ports as shown in Fig.2 for read and write operations [13]. By adding two transistors MN1 and MN2 to the conventional 6T SRAM cell, it separates the read and write operations to address the reduced RSNM problem and thereby increases the transistor count. The read stability of the 8T cell is thus improved compared to conventional 6T cell and provides a read-disturb free operation. Separate read (RWL) and write (WWL) wordlines can be used to access the cell during read and write operations. Read operation is initiated by precharging the read bitline (RBL) HIGH and then read word line (RWL) is asserted to read the stored data in the cell.

However, read bitline leakage is significant particularly in deep submicron ranges. When RBL is not accessed, severe voltage drop occurs at the read bitline due to the leakage current through MN1 and that results in large power dissipation and errors at the output.

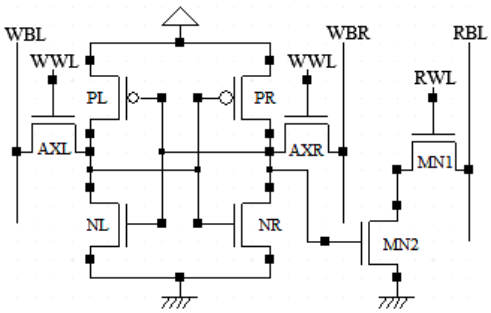

Fig.2. 8T SRAM cell

5. 10T SCHMITT TRIGGER BASED SRAM CELL

Schmitt Trigger (ST) principle can be applied for the cross coupled inverter pair in order to satisfy the conflicting design requirements in conventional SRAM cell [14][15]. Depending upon the direction of input transition, Schmitt Trigger modulates the switching threshold of the inverter using feedback mechanism. In the Schmitt trigger configuration as shown in Fig.3, the transistors MP2 and MN2 have high threshold voltage than MP1 and MN1 due to body bias effect. The addition of two feedback transistors MPF and MNF provides hysteresis such that the output switches from HIGH to LOW or LOW to HIGH only after the ON condition of transistors MN2 or MP2 respectively. Thus the noise immunity of conventional Schmitt Trigger is higher than that of an inverter.

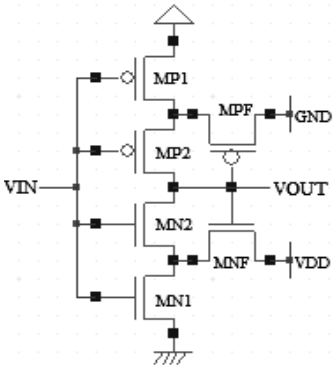

Fig.3.Conventional CMOS Schmitt Trigger

In 10T Schmitt trigger based SRAM cell [16], the feedback mechanism is used only in the pull down path as shown in Fig.4. Transistors P1-N1-N2-NF1 forms one ST inverter while transistors P2-N3-N4-NF2 forms the another Schmitt Trigger inverter of the SRAM cell. Depending upon the direction of input transition, positive feedback from the feedback transistors (NF1/NF2) changes the switching threshold of the inverter.

During 0 to 1 input transition, the feedback transistor (NF1 /NF2) tries to preserve the output at logic HIGH by increasing the source voltage of the pull down transistor (N1/N3). This increases the switching threshold of the inverter and results in sharp transfer characteristics. This leads to robust read operation since read failure is initiated by the 0 to 1 input transition. Thus, the Schmitt Trigger action preserves the logic state of the SRAM cell. Even

though 10T Schmitt Trigger based SRAM cell utilizing differential operation provides better read stability, it has large area overhead compared to conventional 6T SRAM cell.

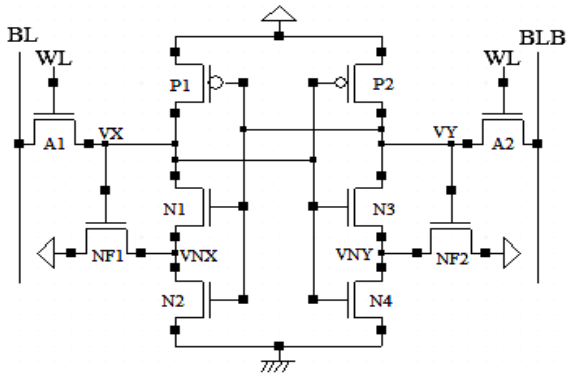

Fig.4. 10T Schmitt Trigger based SRAM cell

6. PROPOSED 8T SCHMITT TRIGGER BASED SRAM DESIGN

6.1 8T ST SRAM CELL

The proposed design aims at making basic inverter pair of SRAM cell efficient for low voltage operations [17]. In the cell shown in Fig.5, PMOS transistors are used as drivers and NMOS transistors are used as pass transistors to access the cell. At low voltages SRAM cell stability is of major concern. 8T ST SRAM cell is used to improve read stability at the expense of speed as PMOS transistors are used as drivers for the cell. Schmitt trigger is used to modulate the switching threshold of the inverter depending on the direction of output transition. This adaption is achieved with the help of a feedback mechanism. In the write operation, in order to write logic "1" to the cell, BL is pulled HIGH and BLB is pulled LOW and vice versa for storing logic"0". Then word line is asserted to turn ON the NMOS access transistors and the values are written into the cell.

During read operation, with *Q*=VDD and *QB*=0, driver transitors *PL*1, *PL*2 are turned ON while *PR*1, *PR*2 turns OFF. To read from the cell, the bitlines are charged to ground and the wordline voltage is asserted to turn on the NMOS access transistors. Here, voltage at node *Q* falls as the bitlines are precharged to ground. Thus, the charges in the bitlines will disturb the data stored in the internal nodes forcing an unintended change in the stored state and leads to read failure. To overcome this problem, feedback mechanism is used to improve switching threshold of the inverter pair. When the voltage at node *Q* falls to $|V_{tp}|$, *PR*2 is ON but *PR*1 is still OFF since PFR is ON and source voltage of *PR*1 is at 0V. Thus, pass transistor feedback mechanism (PFL, PFR) improves the threshold voltages by altering VL and VR node voltages. Thus, the Schmitt trigger operation improves the read stability of the cell and avoids read failure during read mode. RSNM of the SRAM cell is directly proportional to the cell ratio (CR) where CR is defined as the ratio of sizes of storage transistors to the access transistors.

The peripheral circuits of 8T ST SRAM memory includes precharge circuit, Sense amplifier and the write driver circuit.

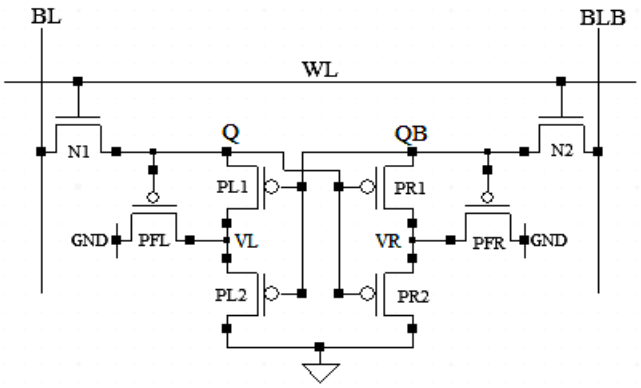

Fig.5. 8T ST SRAM cell

6.2 PRECHARGE CIRCUIT

The precharge circuit used for the 8T Schmitt Trigger based SRAM array is different from that of 6T SRAM array [18]. In the 6T SRAM array, the main function of the precharge circuit is to charge the bitlines to VDD. The bitlines are precharged to ground instead of VDD in the 8T Schmitt Trigger based SRAM array and thus consume less power compared to 6T SRAM array. Fig.6(a) shows the schematic of the precharge circuit for the 6T SRAM array and Fig.6(b) shows schematic of the precharge circuit for the 8T Schmitt Trigger based SRAM array. The precharge signal (PC) enables the bitlines to be precharged during inactive state of the memory cell. The transistor P1 and P2 will precharge the bitlines while P3 will equalize them to ensure both bitlines are at same potential before the cell read operation.

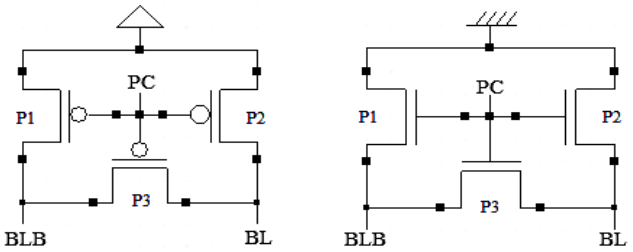

Fig.6. (a). Precharge circuit for 6T SRAM Array (b). Precharge circuit for 8T ST SRAM Array

6.3 SENSE AMPLIFIER

The primary function of a Sense amplifier is to sense the bitline which is being pulled down and amplify the small analog differential voltage to the full swing digital output signal thus performs the read operation of the stored data. Latch type Sense amplifier for the 8T Schmitt Trigger based SRAM array is shown in Fig.7. It has cross coupled latch configuration and the sizing of the transistors is done same as that of the 6T SRAM cell [18]. Read operation begins by precharging and equalizing both the bitlines. The corresponding row is selected by enabling the wordline (WL) to read a particular word from the SRAM array. Sense amplifier is enabled by the read enable signal (RE) when sufficient voltage difference is built between the bitlines. The sense amplifier is used to sense which bitline is heading towards high voltage and which bitline is heading towards ground potential and develops a full voltage swing at the output.

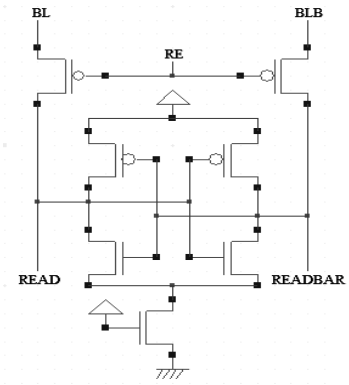

Fig.7. Latch-Type Sense amplifier

6.4 WRITE DRIVER

The main function of the data write circuitry [18] shown in Fig.8 is to write the data to the SRAM cell when write enable signal (WE) is enabled.

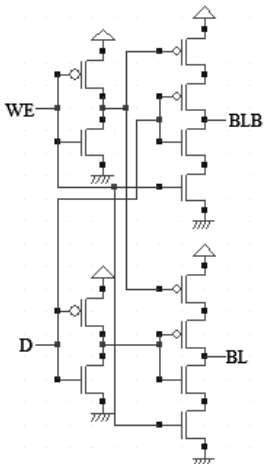

Fig.8. Write Driver circuit

The Fig.9 shows the 8T ST based SRAM cell connected to the peripherals such as write driver circuit, precharge and sense amplifier. During inactive state of the cell, precharge enable signal (PC) is pulled HIGH such that both bitlines BL and BLB are precharged to ground. Precharge circuit is deactivated during the active state of the cell by making the precharge enable signal (PC) LOW. During write operation, write enable signal (WE) and wordlines are made HIGH while the precharge enable signal is made LOW. Sense amplifier is disabled by making read enable signal (RE) of the sense amplifier to HIGH. Data to be written into cell is fed into the datalines such that the data and its complement will be produced at output. Similarly during read operation, sense amplifier is enabled by the read enable signal (RE) to read the data and its complement at READ and READBAR respectively.

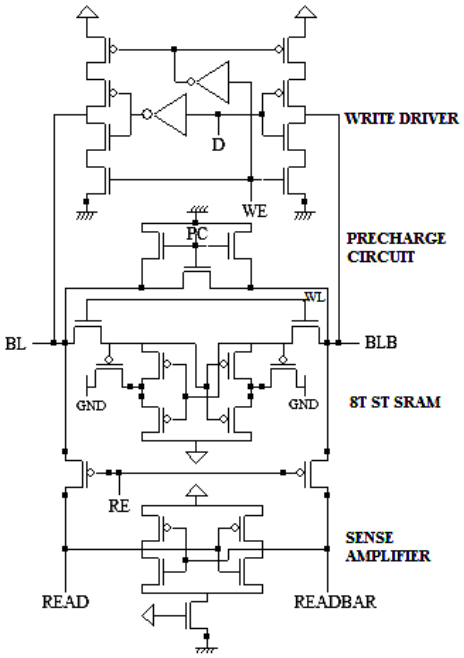

Fig.9. 8T ST SRAM system for reading and writing single bit data

7. SIMULATION RESULTS

The proposed design was simulated in Mentor Graphics ELDO tool based on TSMC 180nm technology. In order to prove the effectiveness of the proposed design, the performance of the proposed design is evaluated against conventional designs. Here, cell properties such as RSNM, area, power consumption are compared with existing designs. The simulation waveform for 8T ST SRAM cell is shown in Fig.10.

7.1 READ STABILITY ANALYSIS

The read stability of the cell is determined by Read Static Noise Margin (RSNM). We measure the RSNM using graphical method. By superimposing VTC of one inverter with VTC of other inverter of the SRAM cell, a two-lobed graph called 'butterfly curve' is obtained such that length of the side of the largest square that can be embedded inside the lobes of the butterfly curve gives the RSNM.

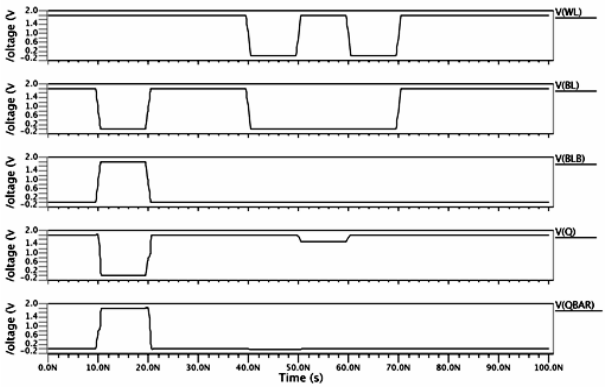

Fig.10. Simulation result for Read/Write operation of 8T ST SRAM cell

The Table.1 shows the RSNM comparison of 8T ST and other SRAM cells at different supply voltages. The RSNM of 8T ST SRAM cell is 2.5× higher than 6T SRAM cell at 1.8V and it can retain data even at lower supply voltage of 0.3V.

Table 1: Supply Voltages VS RSNMs

V_{DD} (V)	RSNM (mV) (6T SRAM)	RSNM (mV) (10T ST SRAM)	RSNM (mV) (8T SRAM)	RSNM (mV) (8T ST SRAM)
1.8	240	370	570	600
1.4	220	350	430	450
1	200	250	390	400
0.6	110	160	200	230
0.4	70	110	120	150
0.3	0 (Read Failure)	40	80	100

From, Fig.11 it is clear that RSNM of 8T ST SRAM is higher than other cells at all supply voltages due to the improved characteristics of the Schmitt Trigger inverter. Thus, from the above results it can be concluded that the 8T ST based SRAM design outperforms conventional designs.

7.2 POWER AND AREA ANALYSIS

The Fig.12 shows the layout view of 8T ST SRAM cell using 120nm technology design rules. Microwind and DSCH was used to get the layout area plots. The Table.2 shows the power and area comparison of different SRAM cell topologies. It is observed that 10T ST SRAM consumes maximum power and area while 8T ST SRAM consumes the minimum power and has reduced area overhead compared to 8T and 10T ST SRAM cells. Thus 8T ST SRAM cell configuration is viable for low power, high density memory designs. From the Table.3 it is clear that the 8T ST based SRAM design has remarkably less power consumption than conventional 6T SRAM design.

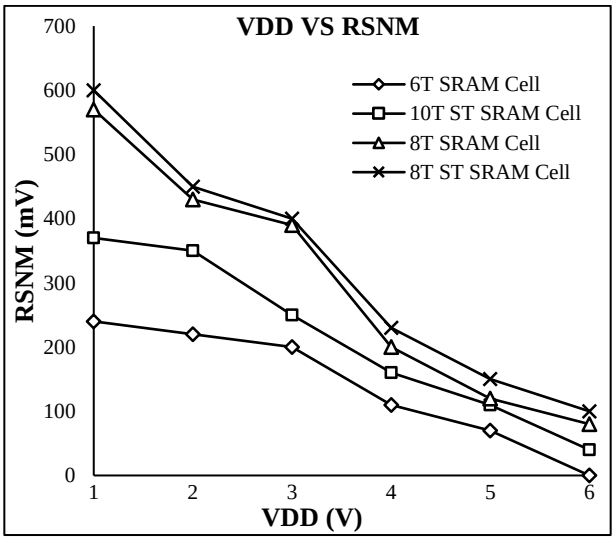

Fig.11. RSNM comparisons at different voltages

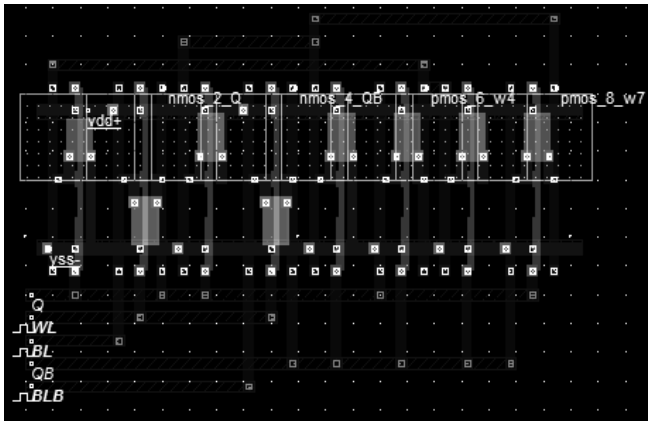

Fig.12. Layout view of 8T ST SRAM cell

Table.2. Comparison of various SRAM cells

SRAM Topologies	Total Power Consumption (pW)	Area (μm^2)
6T Conventional	88.86	13×10 = 130
8T SRAM	92.5	16×11 = 176
10T ST SRAM	129.4	19×11 = 209
8T ST SRAM	69.13	13×12 = 156

Table.3. Power comparison between Single bit 6T and 8T ST SRAM array design

SRAM Cells With peripherals	Total Power Consumption (µW)
6T SRAM	163.97
8T ST SRAM	148.97

8. CONCLUSION

In this paper, an 8T Schmitt Trigger based SRAM cell is introduced that achieves lower power consumption, area and better read stability compared to other SRAM cell topologies. The 8T ST SRAM cell can retain data even at lower supply voltage of 0.3V. This paper has presented a single bit 8T ST SRAM array design with peripheral circuits. Simulation results have shown that 8T ST SRAM design achieves a substantial reduction in power consumption compared to 6T SRAM design. The simulation results have also confirmed that 8T ST SRAM operates with high stability and could be a viable solution for highly dense, low power memory designs.

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